ANSI/TIA/EIA-422-B-1994
Approved: April 13, 1994
Reaffirmed: January 27, 2000
Reaffirmed: September 16, 2005

TIA STANDARD

Electrical Characteristics of Balanced Voltage Digital Interface Circuits

TIA-422-B

(Revision of EIA-422-A)

May 1994

TELECOMMUNICATIONS INDUSTRY ASSOCIATION

Representing the telecommunications industry in association with the Electronic Industries Alliance

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(From Standards Proposal No. 3-4635-RF2, formulated under the cognizance of the TIA TR-30.2 Subcommittee on DTE-DCE Interfaces).

Published by

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Standards and Technology Department
2500 Wilson Boulevard
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FOREWORD

(This foreword is not part of this Standard)

This Standard, from Standards Proposal No. 1849, was formulated under the cognizance of TIA Subcommittee TR-30.2 on Data Transmission Interfaces.

This Standard specifies generators and receivers capable of operating at data signaling rates up to 10 Mbit/s.

No technical changes have been incorporated into TIA/EIA-422-B which will create compatibility problems with equipment conforming to previous versions of TIA/EIA-422. This Standard provides an additional termination option not specified in EIA-422-A. This option is an RC termination, and is optimal for use on low speed control lines where power dissipation is a major concern.

Annex A of this Standard is informative and provides guidelines for application. Annex B of this Standard is also informative and provides information on compatibility with other interface standards, and references to this Standard. Neither Annex is considered part of this Standard.

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ELECTRICAL CHARACTERISTICS OF BALANCED VOLTAGE DIGITAL INTERFACE CIRCUITS

CONTENTS

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1 SCOPE

This Standard specifies the electrical characteristics of the balanced voltage digital interface circuit, normally implemented in integrated circuit technology, that may be employed when specified for the interchange of serial binary signals between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE) or in any point-to-point interconnection of serial binary signals between digital equipment.

This Standard is compatible with ITU-T (Formally CCITT) Recommendation V.11.

The interface circuit includes a generator connected by a balanced interconnecting cable to a load consisting of a receiver or receivers and a termination. The electrical characteristics of the circuit are specified in terms of required voltage, current, and resistance values obtained from direct measurements of the generator and receiver components at the interface points. The logic function of the generator and the receiver is not defined by this Standard, as it is application dependent. The receiver specification for the balanced interface is identical to that specified for the unbalanced interface circuit in TIA/EIA-423-B. Minimum performance requirements for the interconnecting cable are furnished. Guidance is given in Annex A.1 with respect to limitations on data signal rate imposed by the parameters of the cable length, balance, and termination, for individual installations.

The parameter values specified for the balanced generator and load components of the interface are designed such that balanced interface circuits may be used within the same interconnection as unbalanced interface circuits specified by TIA/EIA-423-B. For example, the balanced circuits may be used for data and timing while the unbalanced circuits may be used for low speed control functions.

It is intended that this Standard will be referenced by other standards that specify the complete DTE/DCE interface (e.g., connector, pin assignments, function) for applications where the electrical characteristics of a balanced voltage digital circuit are required. This Standard does not specify other characteristics of the DTE/DCE interface (such as signal quality and timing, etc.) essential for proper operation across the interface.

When this Standard is referenced by other standards or specifications, it should be noted that certain options are available. The preparer of those standards and specifications must determine and specify those optional features that are required for that application.

2 DEFINITIONS

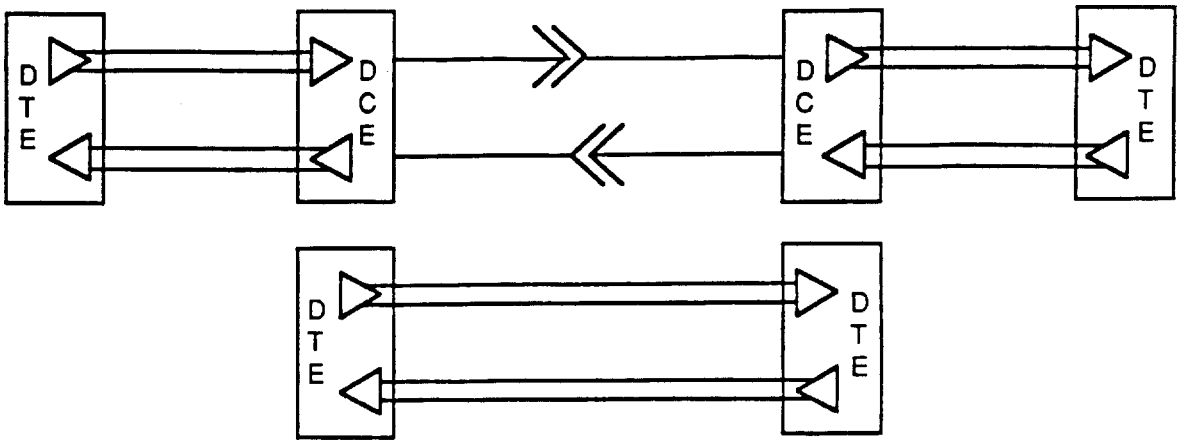
In this Standard, the term:

data signaling rate, expressed in the units bit/s (bits per second), is the significant parameter. It may be different from the equipment's data transfer rate, which employs the same units. Data signaling rate is defined as 1/T where T is the minimum interval between two significant instants. In a binary system for which this Standard is designed, the data signaling rate in bit/s and the modulation rate in bauds are numerically equal when the unit interval used in each determination is the minimum interval. The data signaling rate on the interface lead is different from the equipment's data transfer rate in those systems where modulation establishes a unit interval shorter than the duration of one information bit; such as, in biphase encoded systems where the data signaling rate is twice the data transfer rate.

star (') represents the opposite input condition for a parameter. For example, the symbol Q represents the receiver output state for one input condition, while Q' represents the output state for the opposite input state.

3 APPLICABILITY

The provisions of this Standard may be applied to the circuits employed at the interface between equipments where information being conveyed is in the form of binary signals at the dc baseband level. This Standard shall be referenced by the specifications and specific interface standards applying these electrical characteristics. Typical points of applicability for this Standard are depicted in figure 1.



Legend:

DTE = Data Terminal Equipment

DCE = Data Circuit-Terminating Equipment

= Telecommunications Channel

= Interface Generator

= Interface Receiver

= Balanced Interface Circuit

Figure 1 - Applications of balanced voltage digital interface circuit

The balanced voltage digital interface circuit will normally be utilized on data and timing, or control circuits where the data signaling rate is up to 10 Mbit/s. Balanced voltage digital interface devices meeting the electrical characteristics of this Standard need not operate over the entire data signaling rate range specified. They may be designed to operate over a narrower ranges to satisfy more economically specific applications, particularly at the lower data signaling rates.

While the balanced interface is intended for use at the higher data signaling rates, it may (in preference to the unbalanced interface circuit) generally be required where any of the following conditions prevail:

a. The interconnecting cable is too long for effective unbalanced operation.

b. The interconnecting cable is exposed to extraneous noise sources that may cause an unwanted voltage in excess of ±1V measured differentially between the signal conductor and circuit common at the load end of the cable with a 50 Ω resistor substituted for the generator.

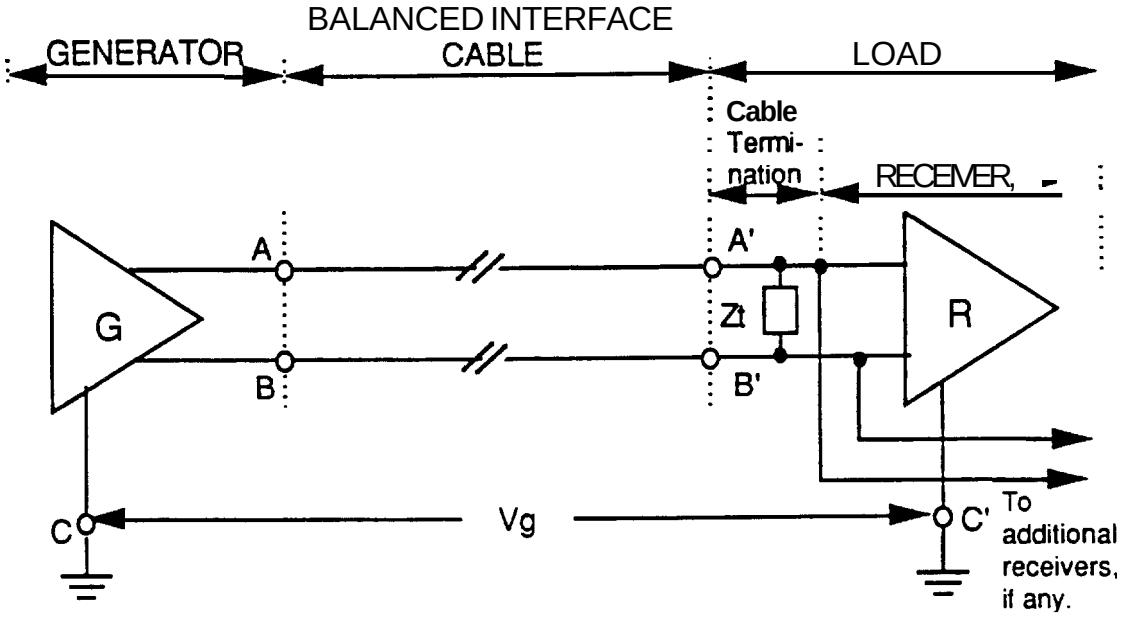
c. It is necessary to minimize interference with other signals.

d. Inversion of the signals may be required; e.g., plus MARK to minus MARK may be obtained by inverting the cable pair.

While a restriction of maximum cable length in not specified, guidelines are given with respect to conservative operating distances as a function of data signaling rate (see Annex A). In general, these conservative values may be greatly exceeded where the installation is engineered to ensure that noise and ground potential values are held within specified limits.

4 ELECTRICAL CHARACTERISTICS

The balanced voltage digital interface circuit is shown in figure 2. The circuit consists of three parts: the generator (G), the balanced interconnecting cable. and the load. The load is composed of one or more receivers (R) and a cable termination (Zt). The electrical characteristics of the generator and receiver are specified in terms of direct electrical measurements while the interconnecting cable is described in terms of its electrical and physical characteristics.



Legend:
G = Generator
R = Receiver
Zt = Termination
Vg = Common Potential Difference
A,B = Generator Interface Points
A',B' = Receiver Interface Points
C = Generator Circuit Common
C' = Receiver Circuit Common

Note: The physical connections of multiple receivers is not defined. See **4.2.5** for recommendations. Termination should be located only at the extreme end of the cable.

Figure 2 - Balanced voltage digital interface circuit

4.1 Generator Characteristics

The generator electrical characteristics are specified in accordance with the measurements illustrated in figures 3 to 8 and described in Paragraphs 4.1.1 through 4.1.6. The generator circuit meeting these requirements results in a low impedance balanced voltage source that will produce a differentia! voltage applied to the interconnecting cable in the range of 2 V to 10 V.

The signaling sense of the voltages appearing across the interconnecting cable are defined in figure 3 as follows:

a. The A terminal of the generator shall be negative with respect to the B terminal for a binary 1 (MARK or OFF) state.

b. The A terminal of the generator shall be positive with respect to the B terminal for a binary 0 (SPACE or ON) state.

The logic function of the generator and the receiver is beyond the scope of this Standard, and therefore is not defined.

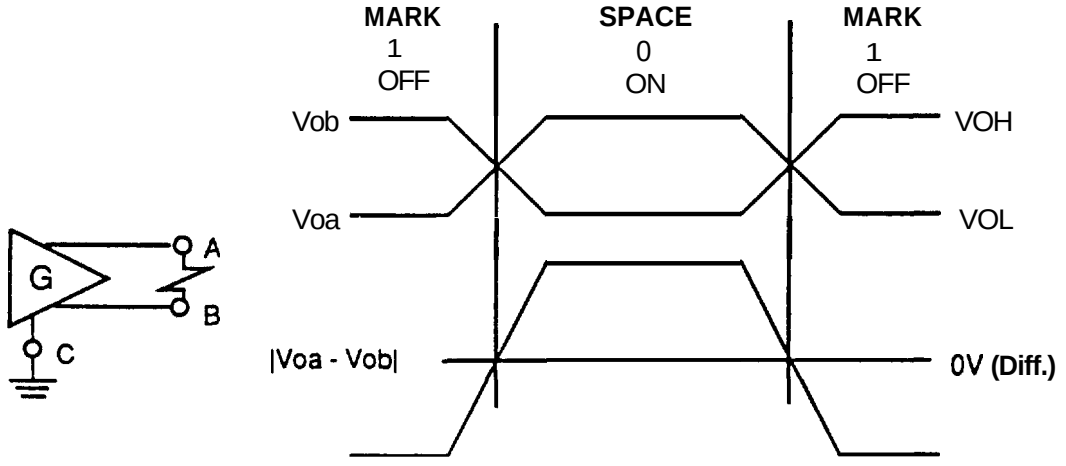


Figure 3 - Signaling sense

4.1.1 Generator Output Impedance

A generator circuit shall present a low impedance of 100 Ω or less between points A and B.

4.1.2 Open Circuit Measurements (Figure 4)

For either binary state, the magnitude of the differential voltage (Vo or Vo') measured between the two generator output terminals shall not exceed **10.0** V. The magnitudes of Voa and Vob respectably, measured with respect to generator circuit common, shall not exceed 6.0 V for either binary state.

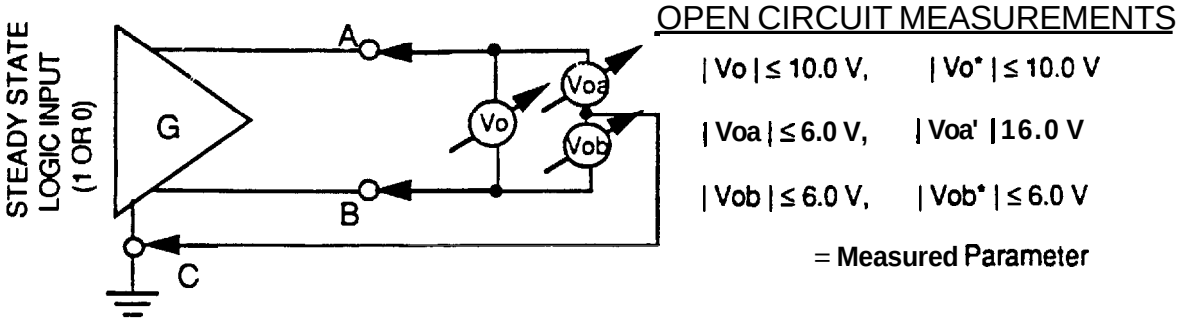


Figure 4 - Open circuit measurements

4.1.3 Test Termination Measurements (Figure 5)

With a test load of two resistors, 49.9 Ω ±1% each, connected in series between the generator output terminals, the magnitude of the differential output voltage (Vt), shall be 2.0 V or greater. For the opposite binary state, the polarity of Vt shall be reversed (Vt'). The magnitude of the difference between Vt and Vt' shall be less than 0.4 V. The magnitude of the generator offset voltage (Vos), measured between the center point of the test load and the generator circuit common shall be 3.0 V or less for either binary state. The magnitude of the difference of Vos for one binary state and Vos' for the opposite binary state shall be 0.4 V or less.

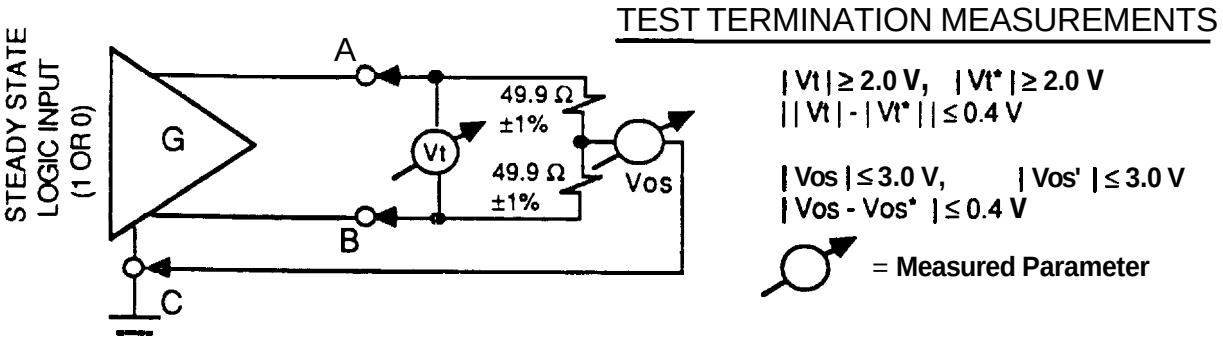


Figure 5 - Test termination measurements

4.1.4 Short-circuit Measurement (Figure 6)

With the generator output terminals short-circuited to the generator circuit common, the magnitudes of the currents (Isa and Isb) following through each output terminal shall not exceed 150 mA for either binary state.

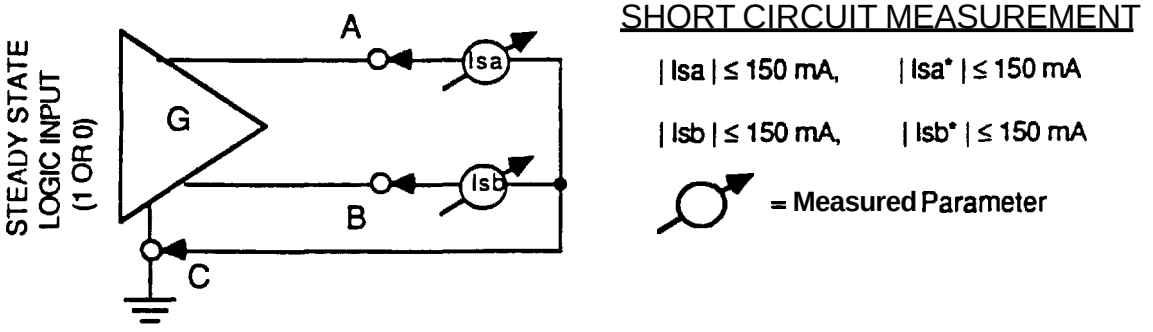


Figure 6 - Short-circuit measurement

4.1.5 Power-off Measurement (Figure 7)

Under the power-off conditions, as defined by the Integrated Circuit manufacturer, the magnitude of the generator output leakage currents (Ixa and Ixb) with voltages ranging from -0.25 V to +6 V applied between each output terminal and generator circuit common, shall not exceed 100 µA.

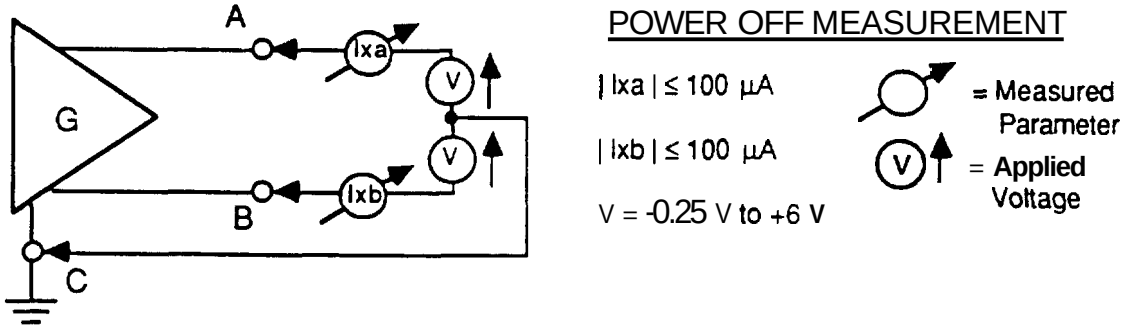
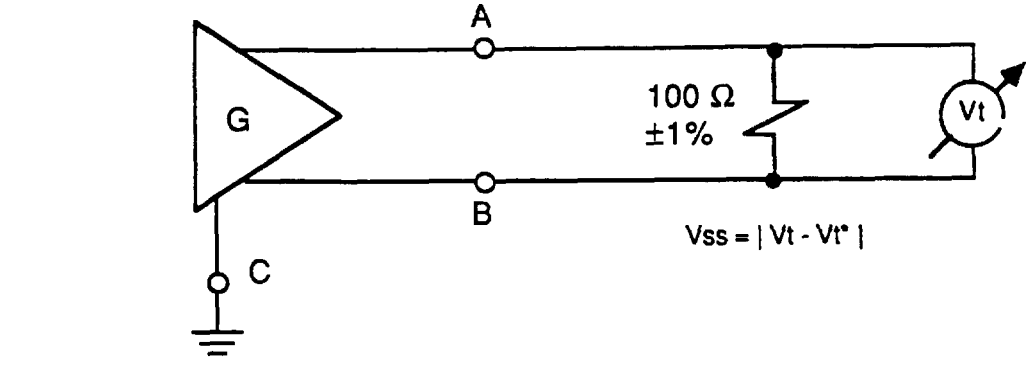


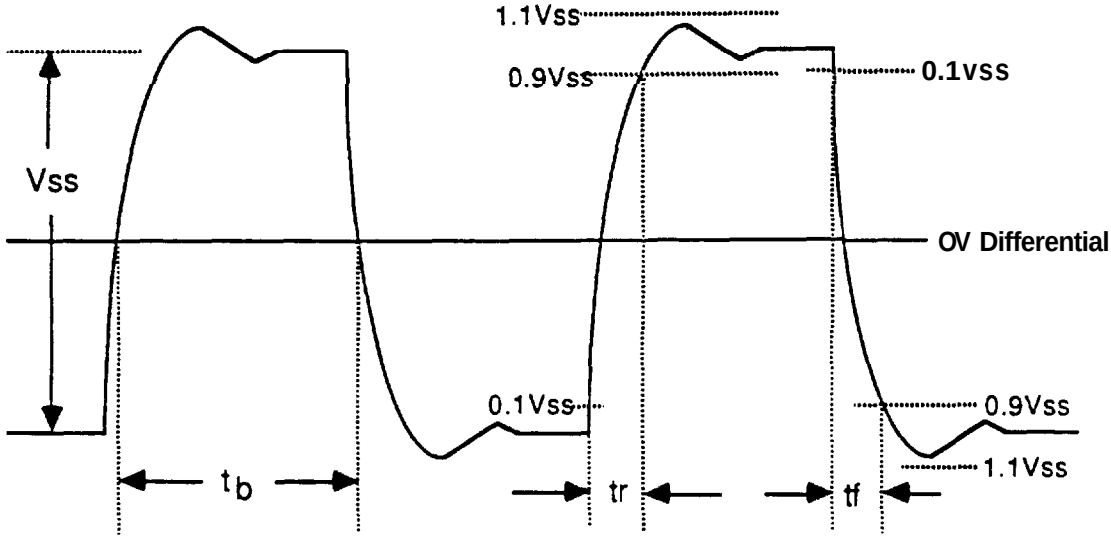
Figure 7 - Power-off Measurement

4.1.6 Output Signal Waveform (Figure 8)

During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the differential voltage measured across a 100 Ω ±1% test load connected between the generator output terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of Vss within 0.1 of the unit interval or 20 ns, whichever is greater. Thereafter, the signal voltage shall

not **vary** more than 10% of Vss from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of Vt or Vt* exceed 10.0 V nor be less than 2.0 V. Vss is defined as the voltage difference between the two steady state values of the generator output.





Legend:

t_b = Time duration of the unit interval at the applicable data **signaling rate.**
$tr \leq 0.1t_b$ when $t_b \geq 200$ ns
$tr \leq 20$ ns when $t_b \leq 200$ ns
Vss = Difference in the steady state voltages
Vss = | Vt - Vt' |

Figure 8 - Output signal waveform

4.2 Load Characteristics

The load is composed of one or more receivers (R) and a termination (Zt) as shown in figure 2. The electrical characteristics of a single receiver without termination or failsafe provision are specified in terms of measurements illustrated in figures 9 to 12 and described in Paragraphs 4.2.1 through 4.2.3.

A circuit meeting these requirements results in a differential receiver having a high input impedance (≥4 kΩ to circuit common), a small input threshold between -0.2 V and +0.2 V, and allowance for an internal bias voltage not to exceed 3 V in magnitude. Multiple receivers and a provision for failsafe operation for specific applications are allowed in the load within the limitations specified in **4.2.7.** The receiver used in the load for the balanced circuit is electrically identical to that specified for the unbalanced interface in TIA/EIA-423-B.

4.2.1 Input Current-Voltage Measurements (Figure 9)

With the voltage Via (or Vib) ranging from +10 V to -10 V while Vib (or Via) is held at OV, the resultant input current Iia (or Iib) shall remain within the shaded region shown in the graph in figure 9. These measurements apply with the receiver's power supply(s) in both power-on and power-off conditions (as defined by the Integrated Circuit manufacturer).

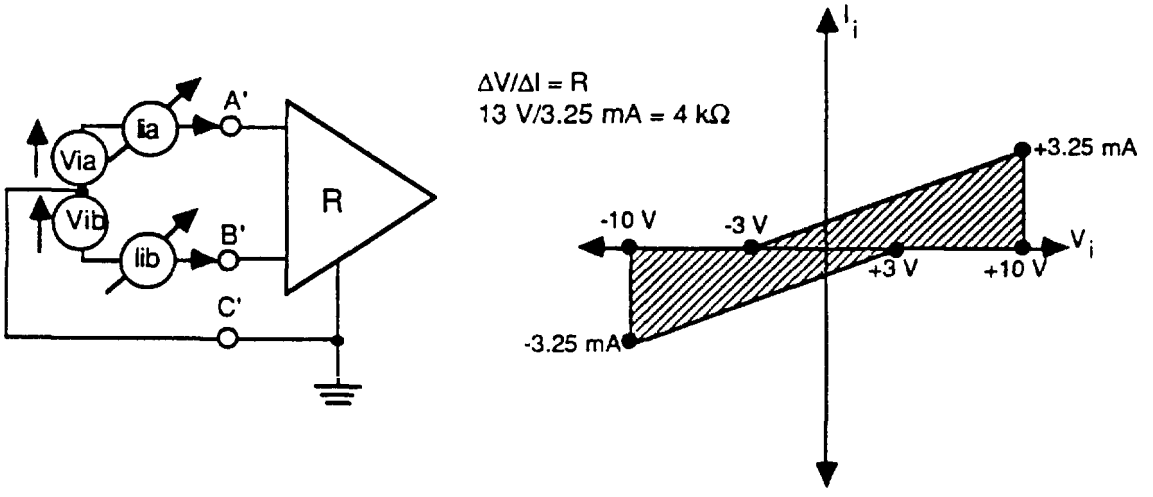


Figure 9 - Receiver input current-voltage measurements

4.2.2 Input Sensitivity Measurements (Figure 10 and 11)

Over an entire common mode voltage (Vcm) range of -7 V to +7 V, the receiver shall not require a differential input voltage of more than | 200 mV | to correctly assume the intended binary state. The common mode voltage (Vcm) is defined as the algebraic mean of the two voltages appearing on the receiver's **input**

terminals (A' and B') with respect to the receiver circuit common (C'). Reversing the polarity of Vi shall cause the receiver to assume the opposite binary state. The receiver is required to maintain correct operation for differential input voltages ranging between 200 mV and 10 V in magnitude. The maximum voltage (signal plus common mode) present between either receiver input and receiver circuit ground shall not exceed 10 V in magnitude, nor cause the receiver to operationally fail. Additionally, the receiver shall operate with a maximum differential of 12 V applied across its input terminals without being damaged.

(NOTE: Designers of terminating hardware should be aware that slow signal transitions with noise present may give rise to instability or oscillatory conditions in the receiver device, and therefore appropriate techniques should be implemented to prevent such behavior. For example, hysteresis may be incorporated into the receiver to help prevent such conditions.)

Figure 11 illustrates the minimum and maximum operating voltages of the receiver. Note, the logic function of the receiver is not defined by this Standard.

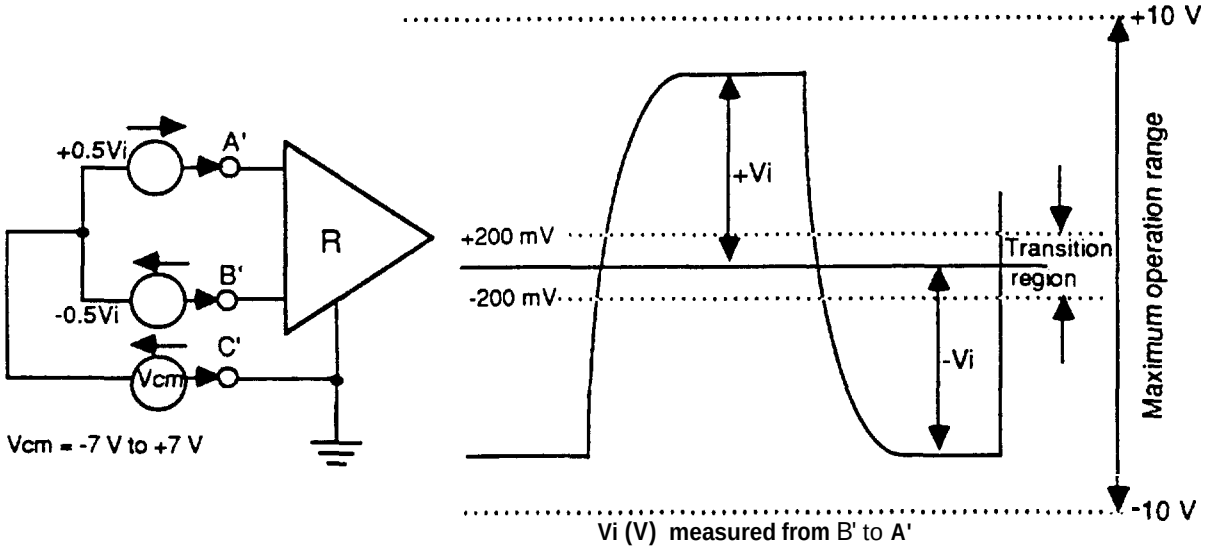
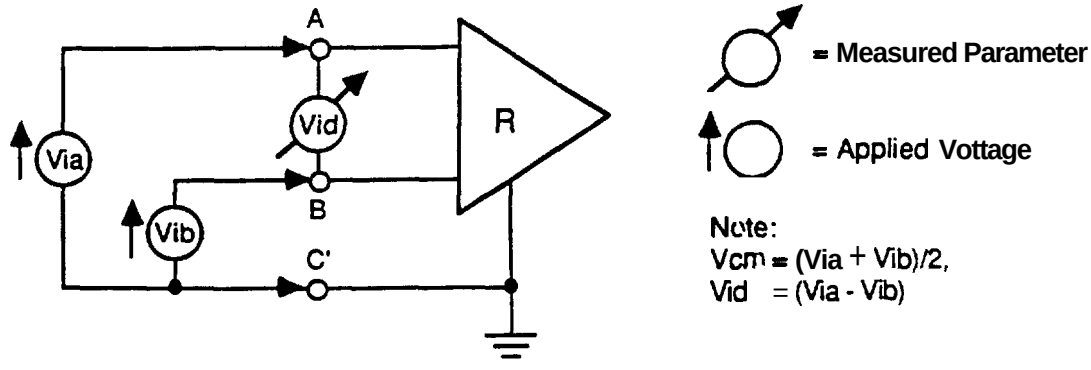


Figure **10** - Input sensitivity measurements



Applied Voltages		Resulting Input Voltage	Resulting Common Mode Voltage	Receiver Output State	Purpose of Measurement
Via	Vib	Vid	Vcm		
-10 V	+2 V	-12 V	-4 V	Q*	To guarantee correct operation with maximum differential voltage applied
+2 V	-10 V	+12 V	-4 V	Q	
+10 V	-2 V	+12 V	+4 V	Q	
-2 V	+10 V	-12 V	4 V	Q*	
+10 V	+4 V	+6 V	+7 V	Q	To guarantee correct operation with maximum common mode voltage applied
+4 V	+10 V	-6 V	+7 V	Q*	
-10 V	-4 V	-6 V	-7 V	Q*	
-4 V	-10 V	+6 V	-7 V	Q	
+0.1 V	-0.1 V	+0.2 V	0 V	Q	200 mV threshold test across common mode range
-0.1 V	+0.1 V	-0.2 V	0 V	Q*	
+7.1 V	+6.9 V	+0.2 V	+7 V	Q	
+6.9 V	+7.1 V	-0.2 V	+7 V	Q*	
-7.1 V	-6.9 V	+0.2 V	-7 V	Q	
-6.9 V	-7.1 V	-0.2 V	-7 V	Q*	

Note: Q is defined as an output state, while Q* is defined as the opposite state.

Figure 11 - Receiver input table

4.2.3 Input Balance Measurements (Figure **12)**

The balance of the receiver input current-voltage characteristics and bias voltage shall be such that the receiver will remain in the intended binary state when a differential voltage (Vi) of more than 400 mV is applied through 499 Ω ±1% to each input terminal, as shown in figure 12, and Vcm is varied between - 7 V to + 7 V. When the polarity of Vi is reversed, the opposite binary state shall be maintained under the same conditions.

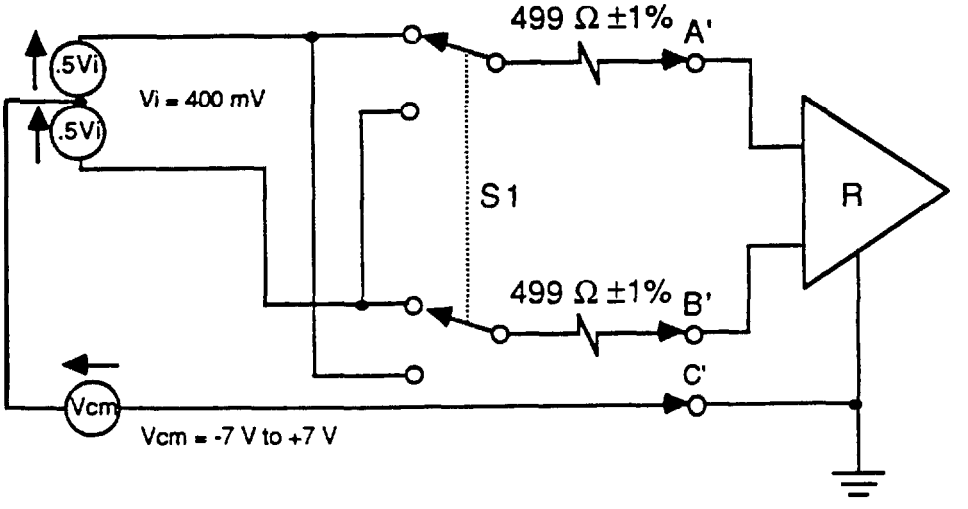


Figure 12 - Input balance measurements

4.2.4 Cable Termination (Figures **13** and 14)

The use of a cable termination is required unless

a) the data rate of the application is less than 200 kbit/s, or

b) the signal rise time at the load end of the cable is greater than four times the one way cable delay (i.e., not a transmission line).

For all other applications, the use of a cable termination is required. Two options are provided.

Option 1 is a resistor connected across the cable normally located at the extreme end of the cable (load end). The value of this resistor (Rt) is in the range of 90 Ω to 150 Ω. Ideally the resistor value is equal to the characteristic impedance of the cable. This termination option is shown in figure 13.

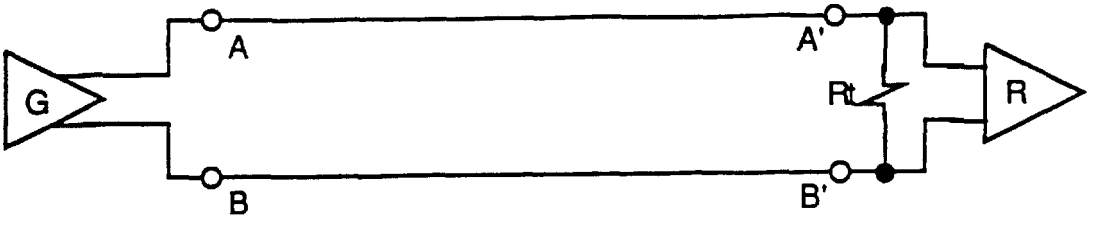


Figure 13 - Resistive termination option

Option 2 is a series connection of a resistor (Rt) and ***a*** capacitor (Ct) (RC Termination) and is connected across the cable at the extreme end of the cable (load end). This termination can be used on low speed control lines and is shown in figure **14.** When power dissipation is a major concern the RC Termination offers a lower power alternative to the standard resistive termination (option 1). The capacitor breaks the dc current loop path, providing a lower power state. The recommended maximum switching rate that should be used with the complex termination is 300 kbit/s, and a maximum cable length of 30 meters (100 feet). The RC Termination can also **be** used on low speed data lines when the time constant (Rt(Ct)) is less than or equal to 1/10 of the unit interval. Exceeding this ratio may cause distortion to the signal waveform.

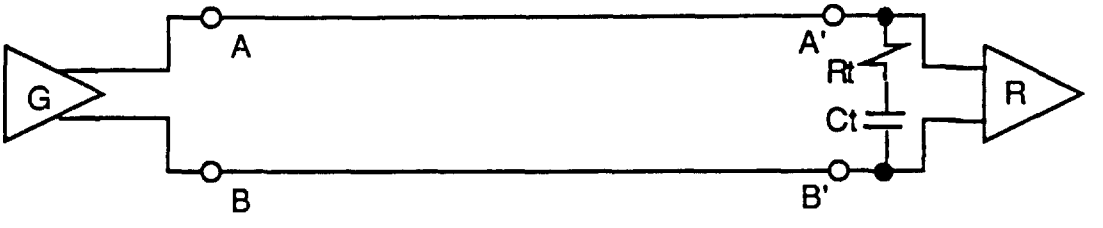
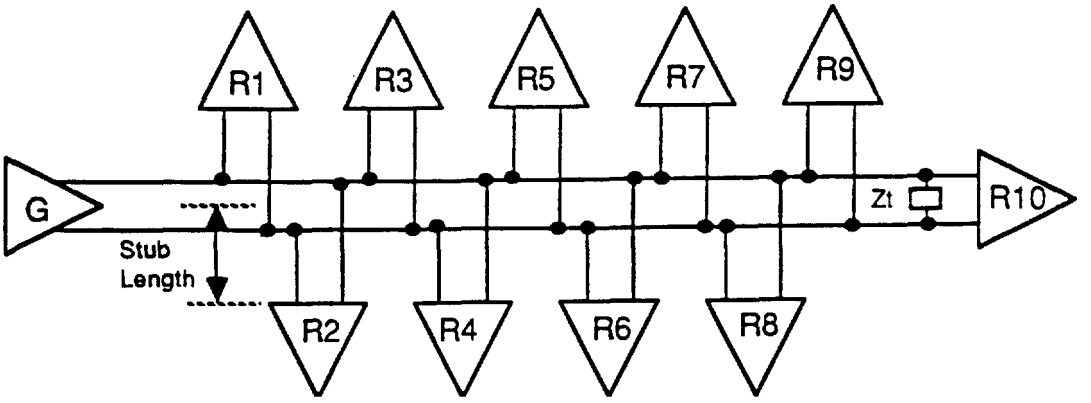


Figure **14 - RC** termination option

See Annex **A** for additional information on cable termination and component values.

4.2.5 Multiple Receiver Operation (Figure **15)**

The driver has the capability to furnish the dc signal necessary to drive 10 parallel connected receivers. However, the physical arrangement of the multiple receivers involves consideration of stub line lengths, fail safe networks, location of the termination, data rate, grounding, etc. that may degrade dynamic characteristics of the load if not properly implemented. It is recommended that stub lengths off **the** main line meet the unterminated requirements of **4.2.4.** The actual arrangement must involve consideration of the aforementioned characteristics for the specific application and is therefore beyond the scope of this Standard. Figure **15** is provided for guidance only.



Note: Stub length off the main-line should be kept as short as possible.

Figure 15 - Multiple receiver operation

4.2.6 Failsafe Operation

Other standards and specifications using the electrical characteristics of the balanced voltage digital interface circuit may require that specific interchange circuits be made failsafe to certain fault conditions. Such fault conditions may include one or more of the following:

1) generator in power-off condition

2) receiver not connected with the generator

3) open-circuited interconnecting cable

4) short-circuited interconnecting cable

5) input signal to the load remaining within the transition region (± 200 mV) for an abnormal period of time (application-dependent)

When detection of one or more of the above fault conditions is required by specified applications, additional provisions are required in the load and the following items must be determined and specified:

1) which interchange circuits require fault detection

2) what faults must be detected

3) what action must be taken when a fault is detected; the binary state that the receiver assumes.

The method of detection of fault conditions is application-dependent and is therefore not further specified.

4.2.7 Total Load Limit

The total load including multiple receivers, fail safe provisions, and cable termination shall have a total resistance greater than 90 Ω between its input points (A' and B', figure 2) or, when a cable termination is not used, the resistance shall be greater than 400 Ω, and shall not require a differential input voltage of more than 200 mV for all receivers to assume the intended binary state.

4.3 Interconnecting Cable Characteristics

The characteristics of the interconnecting cable are not specified. To ensure proper operation, however, paired cable with metallic conductors shall be employed. The performance of any interconnecting cable used must be such as to maintain the necessary signal quality required for the specific application. If necessary for system consideration, shielded cable may be employed (see 7.2). Annex A to this Standard provides guidance on performance and cable length versus data signaling rate.

5 ENVIRONMENTAL CONSTRAINTS

A balanced voltage digital interface circuit conforming to this Standard will perform satisfactorily at data signaling rates up to 10 Mbit/s providing that the following operational constraints are simultaneously satisfied:

a. The interconnecting cable length is within that recommended for the applicable data signaling rate indicated in Annex A and the cable is appropriately terminated.

b. The common mode voltage at the receiver is less than 7 V (peak). The common mode voltage is defined to be any uncompensated combination of generator-receiver common potential difference, the generator offset voltage (Vos), and longitudinally coupled peak noise voltage measured between the receiver's circuit common and cable with the generator's ends of the cable short-circuited to common.

6 CIRCUIT PROTECTION

Balanced voltage digital interface generator and receiver devices, under either the power-on or power-off condition, complying to this Standard shall not be damaged under the following conditions:

a. Generator open-circuit.

b. Short-circuit across the balanced interconnecting cable.

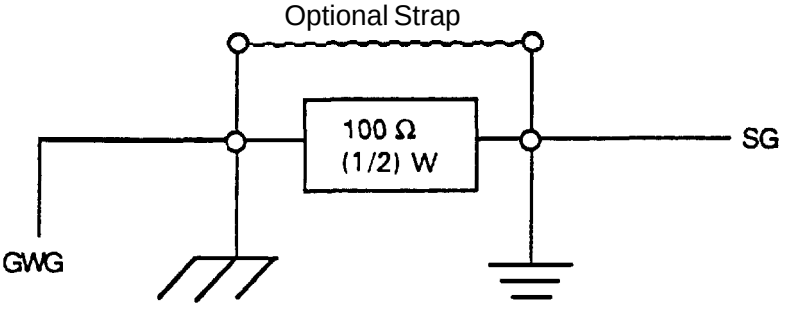
c. Short-circuit to any other lead using electrical characteristics complying to this Standard and TIA/EIA-423-B.

d. Short-circuit to common.

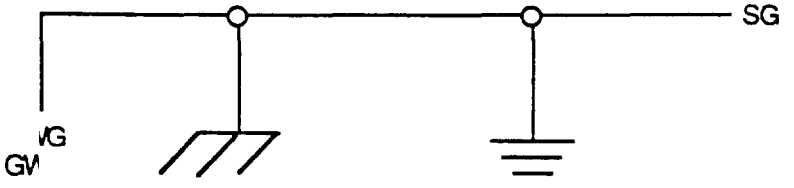
7 OPTIONAL GROUNDING ARRANGEMENTS

7.1 Signal Common (Ground)

Proper operation of the interface circuits, whether using balanced, unbalanced, or a combination of both, requires the presence of a signal common path between the circuit commons of the equipment at each end of the interconnection. The signal common interchange lead shall be connected to the circuit common, which shall be connected to protective ground by any one of the following methods, shown in figure 16, as required by specific application:



Configuration A



Configuration B

Legend:

= Protective ground or frame ground

= Circuit ground or circuit common

SG = Signal ground interchange circuit

GWG = Green wire ground of power system

Figure 16 - Optional grounding arrangements

7.1.1 Configuration "A"

The circuit common of the equipment is connected to protective ground, at one point only, by a 100 Ω, ±20%, resistor with a power dissipation rating of 1/2W. An additional provision may be made for the resistor to be bypassed with a strap to connect signal common and protective ground directly together when specific installation conditions necessitate.

7.1.2 Configuration "B"

The circuit common shall be connected directly to protective ground.

The same configuration need not be used at both ends of an interconnection; however, care should be exercised to prevent establishment of ground loops carrying high currents. (Note: Under certain ground fault conditions in configuration "A", high ground currents may cause the resistor to fail; therefore, a provision shall be made for inspection and replacement of the resistor.)

7.2 Shield Ground

Some interface applications may require the use of shielded interconnecting cable for RFI/EMI or other purposes. When employed, the shield shall be connected only to frame ground at either or both ends depending on the specific application. The means of connection of the shield and any associated connector are beyond the scope of this Standard.

ANNEX A (informative)

GUIDELINES FOR APPLICATION

(This annex is not a formal part of the attached TIA/EIA Recommended Standard, but is included for information purposes only.)

When interconnecting equipment use the electrical characteristics specified in this Standard, consideration should be given to some of the problems that may be encountered due to the interconnecting cable characteristics, cable termination, optional grounding arrangements, fialsafe methods and interconnection with interfaces using other electrical characteristics.

A.1 Interconnecting Cable and Termination

The following information provides further information to **4.3** and is additional guidance concerning operational constraints imposed by the cable parameters of length and termination.

A.1.1 Cable Length with Resistive Termination (Option 1)

The maximum permissible length of cable separating the generator and the load is a function of data signaling rate and is influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and ground potential differences introduced between the generator and the load circuit commons as well as by cable balance. Increasing the physical separation and the interconnecting cable length between the generator and the load interface points increases exposure to common mode noise, signal distortion, and the effects of cable imbalance. Accordingly, users are advised to restrict cable length to a minimum, consistent with the generator-load physical separation requirements.

The curve of cable length versus data signaling rate given in figure A.l may be used as a conservative guide. This curve is based upon empirical data using a **24** AWG, copper conductor, unshielded twisted-pair telephone cable with a shunt capacitance of 52.5 pF/meter (16 pF/foot) terminated in a 100 Ω resistive load. The cable length restriction shown by the curve is based upon assumed load signal quality requirements of:

a. Signal rise and fall times equal to or less than, one-half unit interval at the applicable data switching rate.

b. A maximum voltage loss between generator and load of 66%.

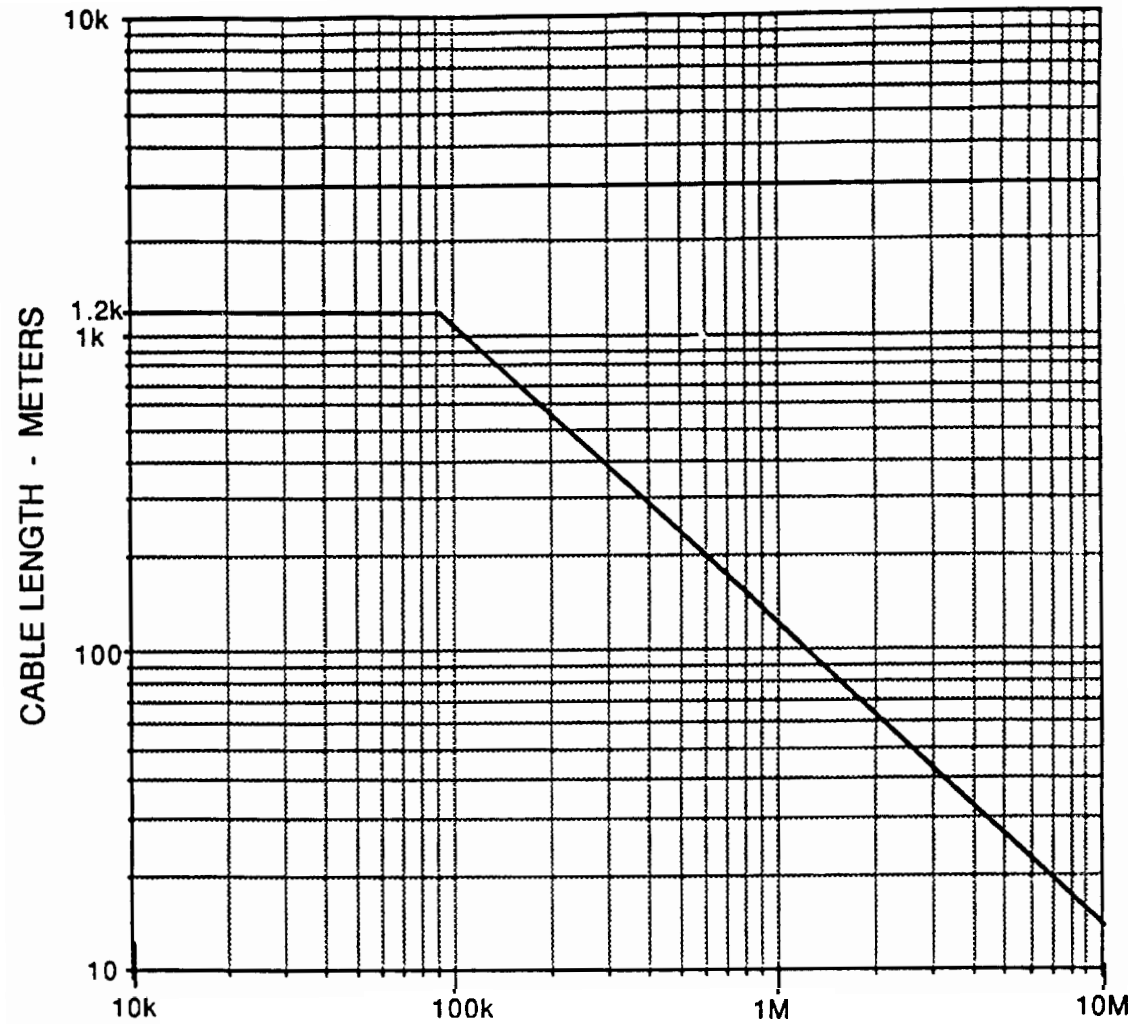


Figure A.1 - Cable length versus data signaling rate

At the higher data signaling rates (90 kbit/s to 10 Mbit/s), the sloping portion of the curve shows the cable length limitation established by the assumed signal rise and fall time requirements. As the data signaling rate is reduced below 90 kbit/s, the cable length has been limited at 1200 meters (4000 feet) by the assumed maximum allowable 66% signal loss.

When generators are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, shall be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the came maximum cable length limits apply).

The user is cautioned that the curve given in figure A.1 does not account for cable imbalance, or common mode noise beyond the limits specified that may be introduced between the generator and the load by exceptionally long cables.

On the other hand, while signal quality degradation within the bounds of figure **A.I** will ensure a zero crossing ambiguity of less than 0.5 unit interval, many applications can tolerate greater timing and amplitude distortion. Thus, correspondingly greater cable length may be employed than those indicated. Experience has shown that, in most practical cases, the operating distance at lower data rates signaling rates may be extended to several kilometers.

Cables having characteristics different from the twisted pair **24** AWG, 52.5 pF/meter (16 pF/foot), can also be employed within in bounds of figure **A.1.** First, determine the absolute loop resistance and capacitance values of the typical **24 AWG** cable provided by the cable length associated with the data signaling rate desired from figure **A.1.** Then convert those values to equivalent lengths of the cable actually used. For example, longer distances would be possible when using 19 AWG, while shorter distances would be necessary for **28 AWG.**

The type and length of the cable used must be capable of maintaining the necessary signal quality needed for the particular application. Furthermore, the cable balance must be such as to maintain acceptable crosstalk levels, both generated and received.

A.1.2 Cable Termination

The characteristic impedance of twisted pair cable is a function of frequency, wire size and type as well as the kind of insulating materials employed. For example, the characteristic impedance of average **24** AWG, copper conductor, plastic insulated unshielded twisted-pair cable, to a **100-kHz** sine wave will be on the order of **100 R.**

In. general, reliable operation of the balanced interface circuit is not particularly sensitive to the presence or absence of the cable termination at lower speeds (below **200** kbit/s) or at any speed where the signal rise time at the load end of the cable is greater than **4** times the one-way propagation delay time of the cable.

At other speeds and distances cable termination is required. Two options exist with option **1** being more common, and option 2 ideal for use on low speed control lines. Option **1** is a resistor ranging from 90 **R** to **150 Ω** and is connected across the cable at the load end. Ideally, Rt is selected to match the characteristic impedance of the cable (Zo) to minimize reflections. Option 2 is a series connection of a capacitor and a resistor and is connected across the cable at the load end. The resistor should be in the range of **90 Ω** to **150 R** and is selected to match the characteristic impedance of the cable (Zo).

The capacitor is selected to be equal to the round trip delay of the cable divided by the characteristic impedance of the cable. Additionally the RC time constant should be less than or equal to 0.1 of the unit interval (tb).

Ct = (Cable Round Trip Delay)/ Zo

where:

Ct = DC Isolation Capacitor (Termination Capacitor)
Zo = Characteristic impedance of the Cable

In an example case of a 30 meter (100 foot) cable with characteristic impedance of 100 Ω, the method to select the capacitor (Ct) value is the following:

(1) Cable Round Trip Delay = (30 meter) (2) (5.67 ns/m) = 340 ns

(2) Ct = (340 ns)/(100 Ω) = 3,400 pF

However, the RC time constant of Rt(Ct) should be ≤ 1/10 of the unit interval.

(3) Rt(Ct) = 100 Ω (3,400 pF) = 340 ns

(4) Minimum Unit Interval = 10 (340 ns) = 3.4 µs => 300 kbit/s

The maximum recommended data rate for the 30 meter (100 foot) cable example is 300 kbit/s or slower.

A.2 Codirectional and Contradirectional Timing Information

With codirectional (same direction as data) timing, there are minimal problems with proper clocking of the data bits since the difference between data and clock edges is mostly the result of generator and receiver skew and not the transmission line. With contradirectional timing, the user is advised that generator and receiver skew are not the only items to be taken into account. The cable delay and skew must also be considered. In both cases the clock should transition as close to the center of the data bit as possible.

ANNEX B (informative)

B.I Compatibility With Other Interface Standards

As stated in the scope of signaling, generators and receivers meeting the requirements of TINEIA-422-B are compatible with those meeting ITU-T (Formally CCITT) Recommendation V.II. The electrical characteristics of the balanced voltage digital interface are designed to allow both balanced and unbalanced (see TINEIA-423-B) circuits within the same interconnection cable sheath. For example, the balanced circuits may be used for data and timing while the unbalanced circuits may be used for low speed control functions.

Since the basic differential receivers of TINEIA-422-B and TINEIA-423-B are electrically identical, it is possible to interconnect equipment using TIA/EIA-423-B receivers and generators on one side of the interface with equipment using TIA/EIA-422-B generators and receivers on the other side of the interface, the leads of the balanced receivers and generators are properly configured to accommodate such an arrangement and the cable is not terminated.

The balanced interface circuit is not intended for interoperation with other interface electrical characteristics such as EIA/TIA-232-E, MIL-STD-188C, MIL-STD-188-114 (type 1), and ITU-T (Formally CCITT) Recommendation V.28. Under certain conditions, interoperation with circuits of some of the above interfaces may be possible but may require modification in the interface or within the equipment; therefore, satisfactory operation is not assured, and additional provisions not specified herein may be required.

B.2 RELATED TIA/EIA STANDARDS

EIA-334-A, SIGNAL QUALITY AT INTERFACE BETWEEN DATA TERMINAL EQUIPMENT AND SYNCHRONOUS DATA CIRCUIT-TERMINATING EQUIPMENT FOR SERIAL DATA TRANSMISSION

EIA-363, STANDARD FOR SPECIFYING SIGNAL QUALITY FOR TRANSMITTING AND RECEIVING DATA PROCESSING TERMINAL EQUIPMENTS USING SERIAL DATA TRANSMISSION AT THE INTERFACE WITH NON-SYNCHRONOUS DATA COMMUNICATIONS EQUIPMENT

EIA-404-A, STANDARD FOR START-STOP SIGNAL QUALITY FOR NON-SYNCHRONOUS DATA TERMINAL EQUIPMENT

TIA/E*IA-423-B, ELECTRICAL CHARACTERISTICS OF UNBALANCED VOLTAGE DIGITAL INTERFACE CIRCUITS*

ANSI/EIA/TIA-530-A-1992, *HIGH SPEED 25-POSITION INTERFACE FOR DATA TERMINAL EQUIPMENT AND DATA CIRCUIT-TERMINATING EQUIPMENT, INCLUDING ALTERNATIVE 26-POSITION CONNECTOR*